Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **NC**
2. **INPUT**
3. **TEMP**
4. **GND**
5. **TRIM**
6. **OUTPUT**
7. **HEATER**
8. **NC**

**.072”**

**.084”**

**7**

**1019B**

**MASK**

**REF**

**6**

**5**

**4**

**2**

**3**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size = .004” X .004”**

**Backside Potential:**

**Mask Ref: 1019B**

**APPROVED BY: DK DIE SIZE .072” X .084” DATE: 8/21/19**

**MFG: LINEAR TECHNOLOGY THICKNESS .012” P/N: LT1019**

**DG 10.1.2**

#### Rev B, 7/1